REMARKS

Claims 1-21 are pending. In view of the following, all pending claims are in condition for allowance. If, after considering this response, the Examiner does not agree that all of the claims are allowable, he is requested to schedule a teleconference with the Applicants' attorney to further the prosecution of the application.

Rejection of claims 1-2, 5, 9-10, 12-17 and 19-21 under §103(a) as being unpatentable over Pittelkow et al (US 6,996,741) in view of Chow et al. (US 2002/0069317)

Claim 1

Claim 1 recites circuit means, functionally independent, each of them being responsible for the correction of a predetermined storage error of data stored in a non-volatile solid-state memory.

For example, referring, *e.g.*, to paragraphs 2, 4, 10-12 and 36-39 of the present application, circuit means are responsible for the correction of a predetermined storage error of data stored in a non-volatile solid-state memory 2. Specifically, the non-volatile solid-state memory 2 may be a flash-type memory. It should be noted that the non-volatile solid-state memory 2 is the primary data-storage unit of memory system 1. It should be further noted that all error correction is for data stored in the non-volatile solid-state memory 2.

Pittelkow, on the other hand, does not disclose circuit means, functionally independent, each of them being responsible for the correction of a predetermined storage error of data stored in a non-volatile solid-state memory. Instead, Pittelkow discloses a storage area network (SAN) controller 102, 201 for controlling access to disk drives 110a-110d (FIGS. 1 and 2; col. 5, line 30 – col. 8, line 17). However, disk drives 110a-110d are simply conventional disk drives, which are completely different from solid-state memory. Solid-state memory such as NVRAM 228 is only used in Pittelkow to "retain a copy of the storage configuration information" of the system, not as the primary data-storage unit of the system (col. 7, lines 43-47). Furthermore, not only

is no automatic error correction ever performed on the actual data stored in solid-state memory such as NVRAM 228, but no automatic error correction is ever performed on the actual data stored in the conventional disk drives 110a-110d either. The only failures disclosed in Pittelkow are described under the headings "External Devices", "Internal Resources", and "Failure Manager" (col. 23, line 15 – col. 26, line 27). Under the heading "External Resources", Pittelkow discloses determining whether the controller 201 itself has suffered a sever failure, or whether the controller 210 itself is going off-line (col. 23, lines 18-28). However, Pittelkow does not disclose performing automatic error correction on the actual data stored in the conventional disk drives 110a-110d or in the solid state memory 228. Under the heading "Internal Resources", Pittelkow discloses monitoring the health of components inside the controller 201 itself, specifically the CCB 201 and the processors 208 and 212 (col. 23, lines 43-64). However, Pittelkow does not disclose performing automatic error correction on the actual data stored in the conventional disk drives 110a-110d or in the solid state memory 228. Under the heading "Failure Manager", Pittelkow discloses a list of failures that can occur inside the controller 201 itself, or between a $controller_1$ and a $controller_2$ connected by an Ethernet link 8 (col. 24, line 24 – col. 26, line 27). However, Pittelkow does not disclose performing automatic error correction on the actual data stored in the conventional disk drives 110a-110d or in the solid state memory 228. In fact, after reviewing Pittelkow in its entirety, the Applicants' attorney is unable to find any mention of performing automatic error correction on data stored in the conventional disk drives or in the solid-state memory.

Similarly, Chow does not disclose circuit means, functionally independent, each of them being responsible for the correction of a predetermined storage error of data stored in a non-volatile solid-state memory. Instead, Chow simply discloses the use of solid-state drives (paragraph [0010]). However, this has nothing to do with the automatic correction of a predetermined storage error of data stored in the memory. Chow simply does not disclose the shortcomings of Pittelkow in any way.

Therefore, the combination of Pittelkow and Chow does not satisfy all of the limitations of claim 1.

Claims 9, 17, 19 and 21

Claim 9, 17, 19 and 21 are patentable for reasons similar to those recited above in support of the patentability of claim 1.

Claims 2, 5, 10, 12-16 and 20

Claims 2, 5, 10, 12-16 and 20 are patentable by virtue of their respective dependencies from claims 1, 9 and 19.

Rejection of claims 3-4, 6-8, 11 and 18 under §103(a) as being unpatentable over Pittelkow and Chow in view of Saxena et al. (US 5,533,035)

Claims 3-4, 6-8, 11 and 18 are patentable by virtue of their respective dependencies from claims 1, 9 and 17.

CONCLUSION

In light of the foregoing, claims 1-21 are in condition for allowance, which is respectfully requested.

If the Examiner determines that additional fees are necessary, he is authorized to charge them to deposit account number 07-1897.

If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner schedule a phone interview with the Applicants' attorney at (425) 455-5575.

Dated this 10th day of March, 2008.

Respectfully submitted,

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